Q2 Known Good Substrates Technical Report
CONTRACT/PR NO. N00014-08-C-0398 Dow Corning Corporation
Quarterly Technical Report
Reporting Period: 1 January – 31 March 2009

Executive Summary

By quarter 2 of the program, most all subcontractors are under contract and technical progress is starting to develop. All subcontractors have received wafers and are in the device fabrication process.

Technical Progress

The following table documents the key program end metric goals.

Metric	50th Percentile	20th Percentile
MPD distribution 4H n+ 76 mm diameter (cm^{-2})	2	<2
MPD distribution 4H n+ 100 mm diameter (cm^{-2})	10	5
Net scratch length by LLS relative to wafer diameter (%)	30	15
Equivalent Epitaxy Defect Density 76mm diameter (cm^{-2})	<5	<3
Epitaxy Doping Target Accuracy	+/- 15%	+/-10%
Epitaxy Doping Variation within wafer (Max-Min/Min, %)	25%	10%
Substrate Resistivity Maximum 4H n+ all diameters	0.020	0.018

The table is now color coded to reflect the status of the program. Green=met goal; yellow=nearly met; red=not met. Details and data pertinent to the specific goals are provided in the next section of the report.

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14. ABSTRACT
The Known Good Substrates (KGS) Phase III program was initiated 29 September 2008. Wafer, epitaxy, modeling and metrology work has been the main focus of efforts in Q2. This technical report summarizes the progress by all team members against the tasks and milestones.

15. SUBJECT TERMS
SiC wafer, SiC epitaxy, SiC material metrology

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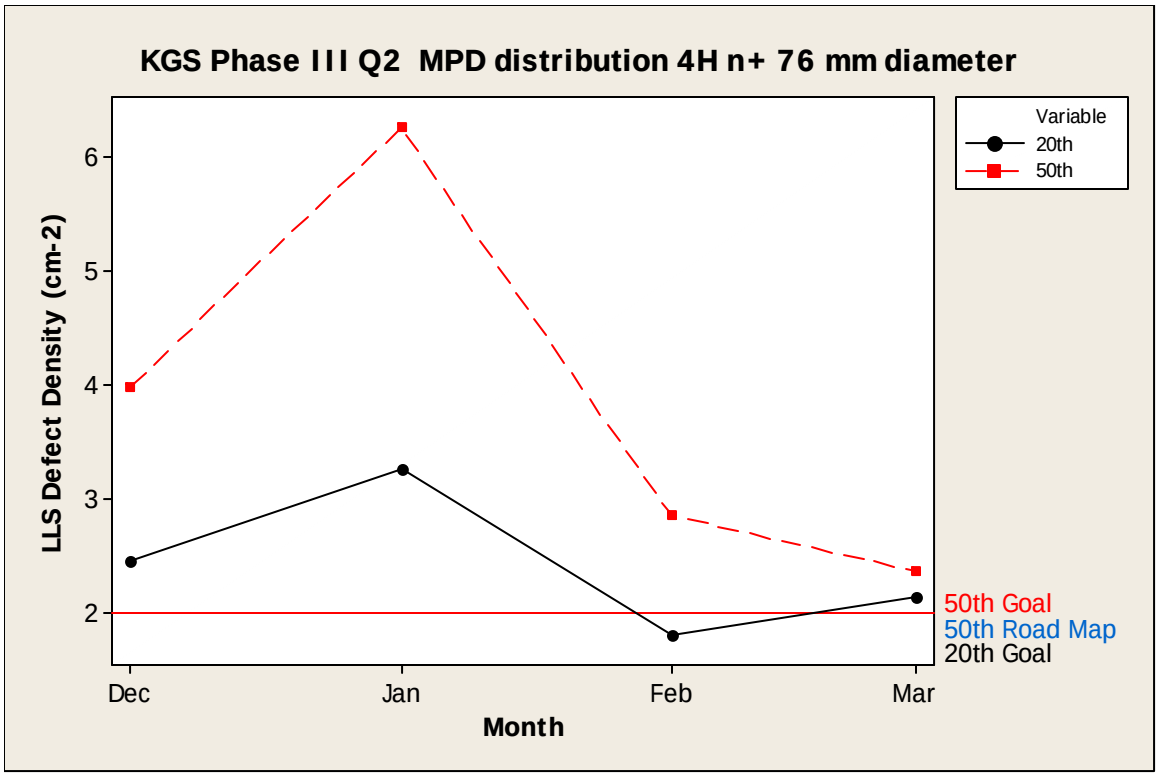
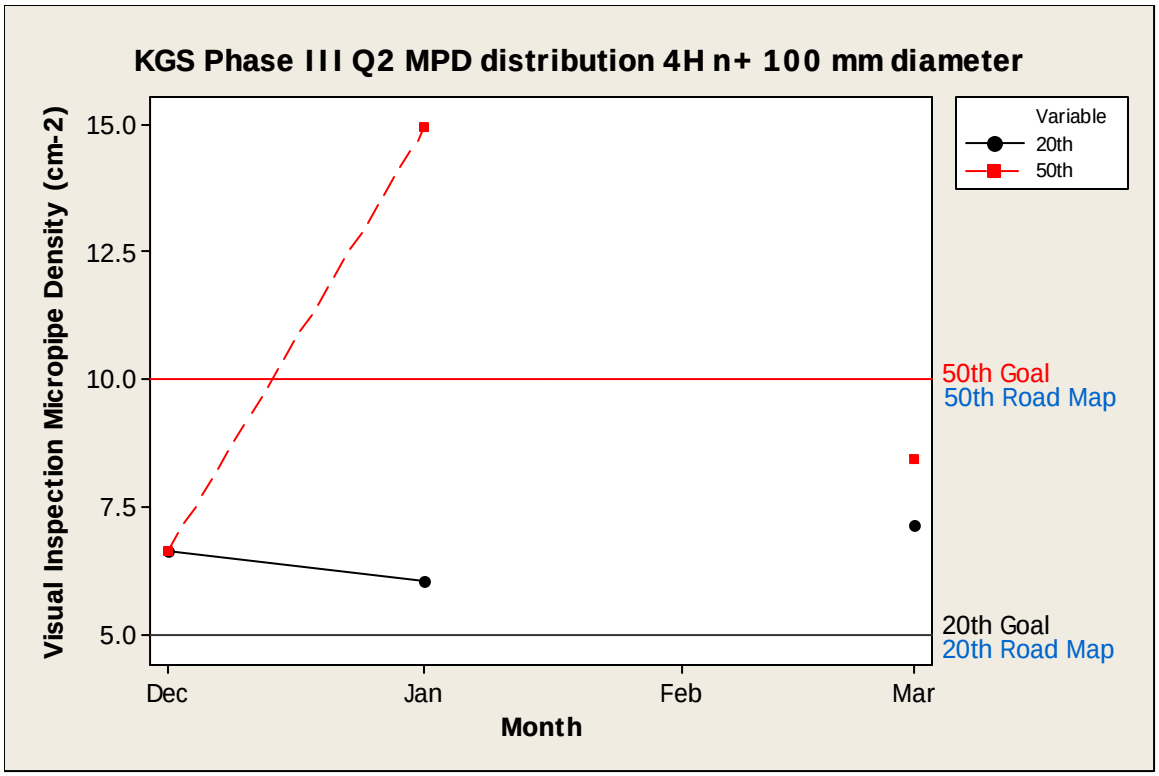
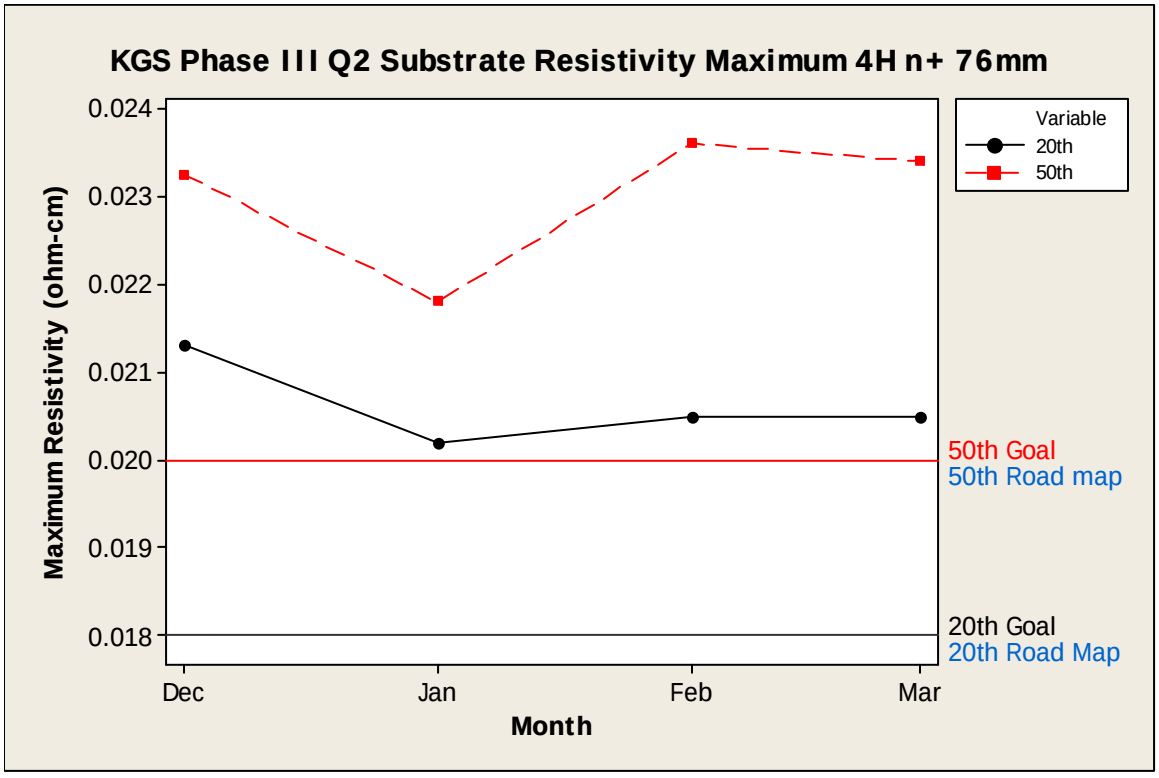
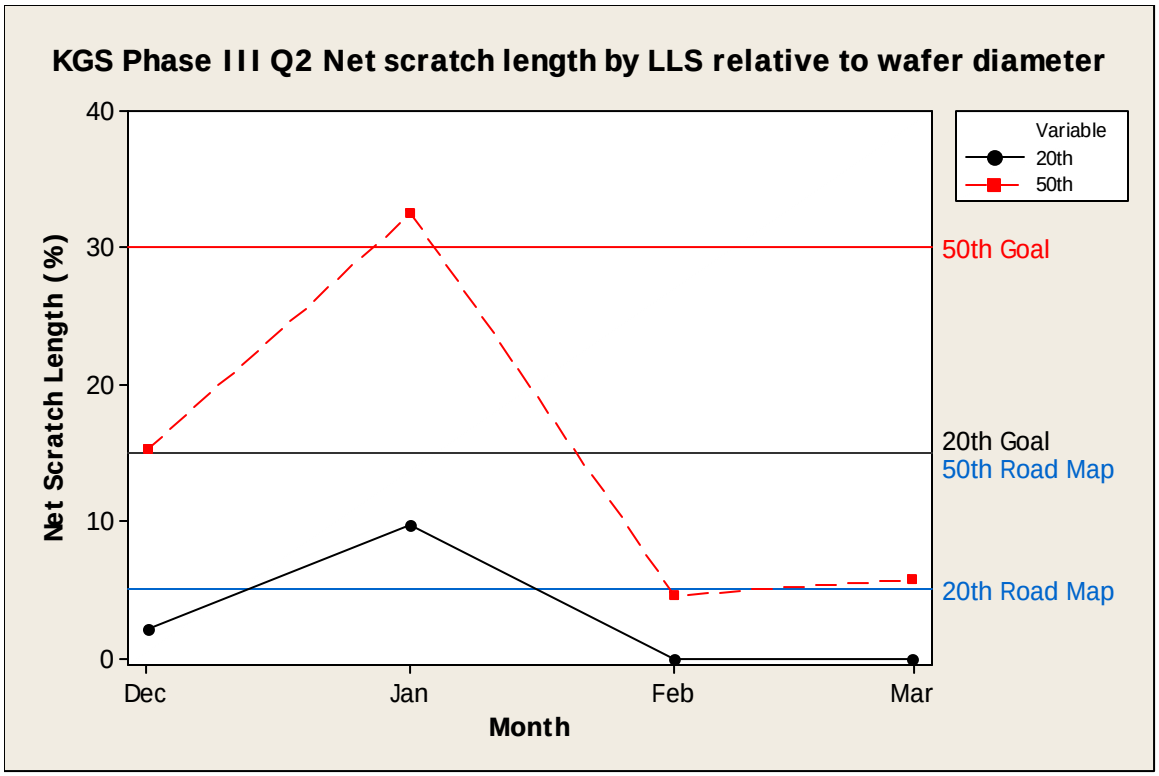
Progress against Metrics – Percentile Values

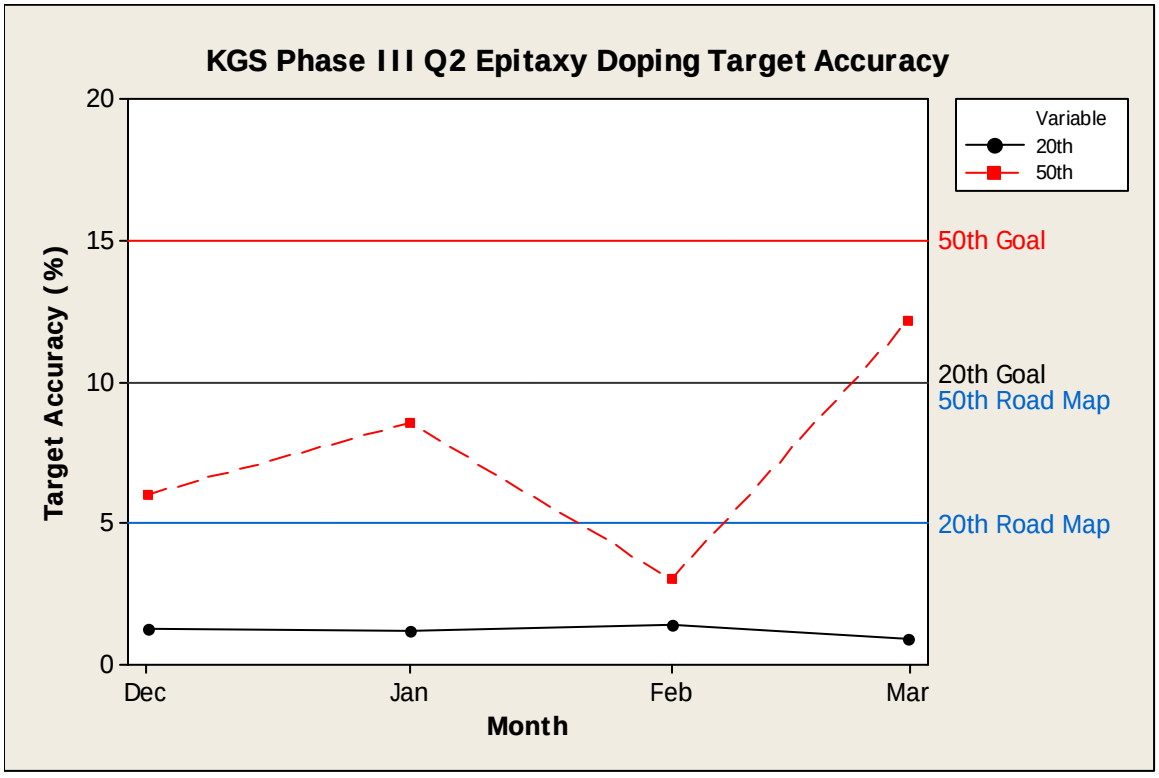
In addition to the program metrics, charts also show roadmap metric targets which were developed during discussions with partners during the Jan 2009 KGS II Review meeting.

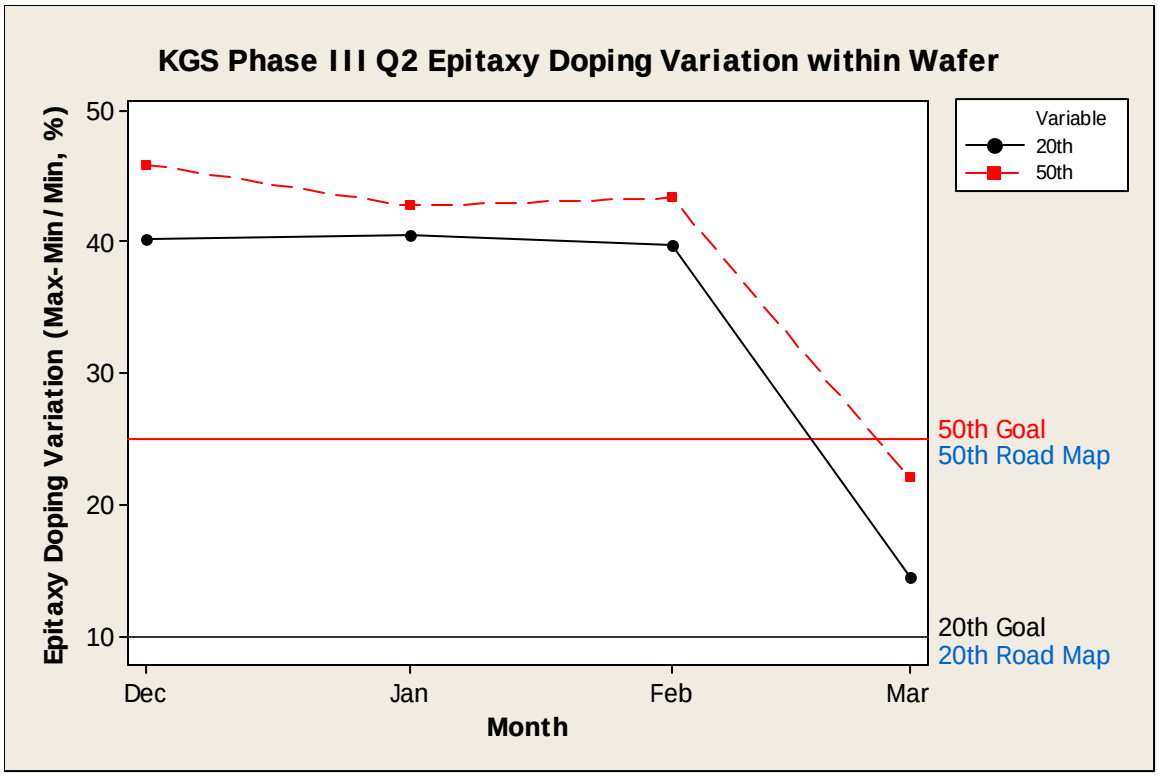


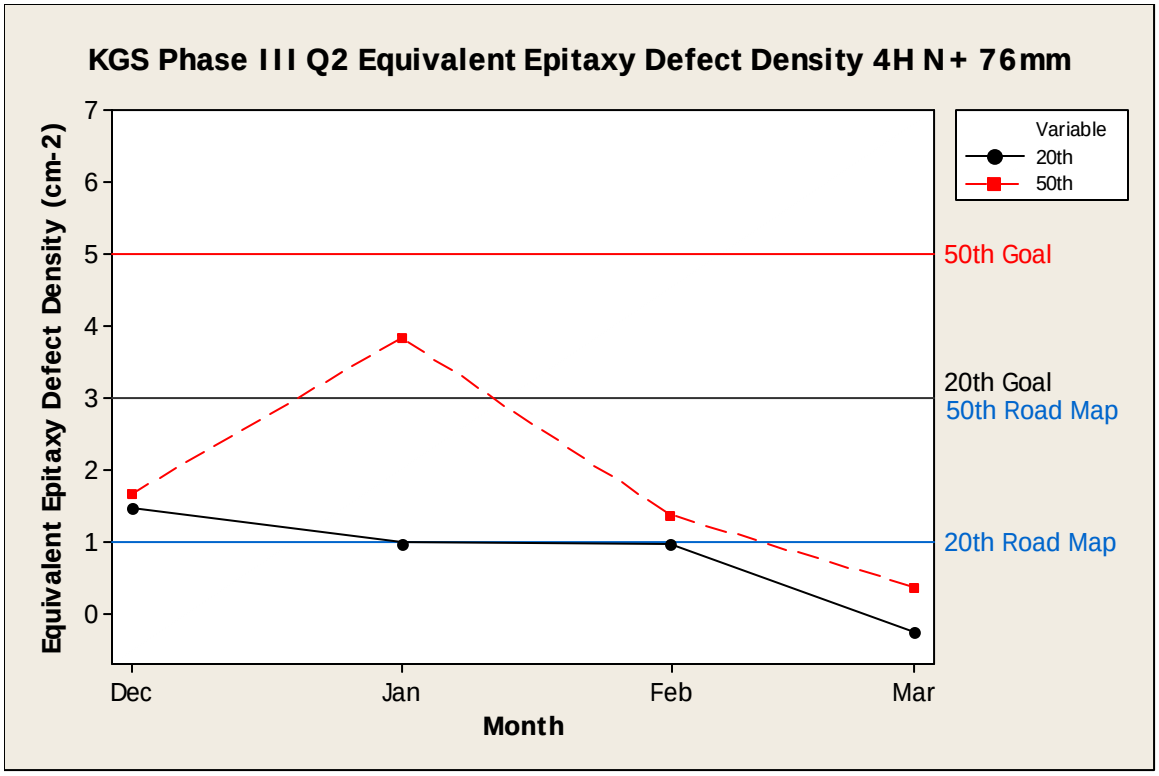

KGS Phase III Q2 MPD distribution 4H n+ 100 mm diameter
Visual Inspection Micropipe Density (cm-2)
15.0
12.5
10.0
7.5
5.0
Dec
Jan
Feb
Mar
Month
Variable
20th
50th
50th Goal
50th Road Map
20th Goal
20th Road Map


KGS Phase III Q2 Substrate Resistivity Maximum 4H n+ 76mm
Maximum Resistivity (ohm-cm)
0.024
0.023
0.022
0.021
0.020
0.019
0.018
Dec
Jan
Feb
Mar
Month
Variable
20th
50th
50th Goal
50th Road map
20th Goal
20th Road Map

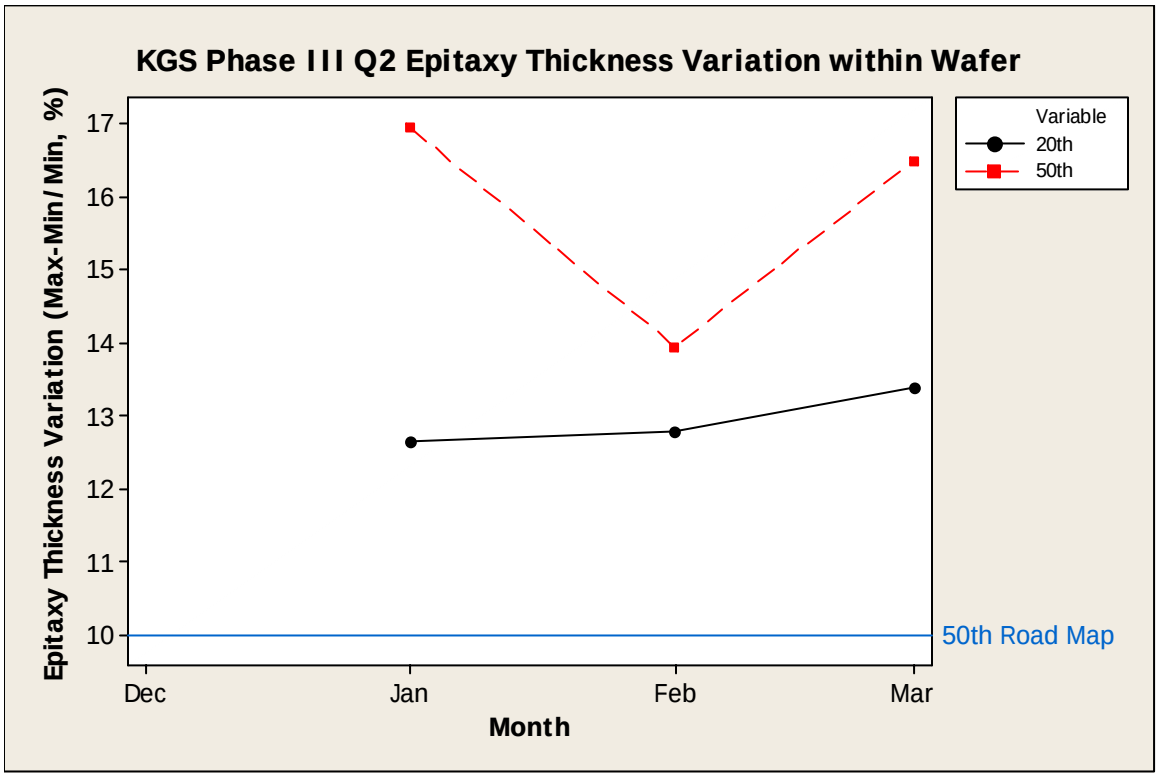

KGS Phase III Q2 Net scratch length by LLS relative to wafer diameter
Net Scratch Length (%)
40
30
20
10
0
Dec
Jan
Feb
Mar
Month
Variable
20th
50th
50th Goal
20th Goal
50th Road Map
20th Road Map

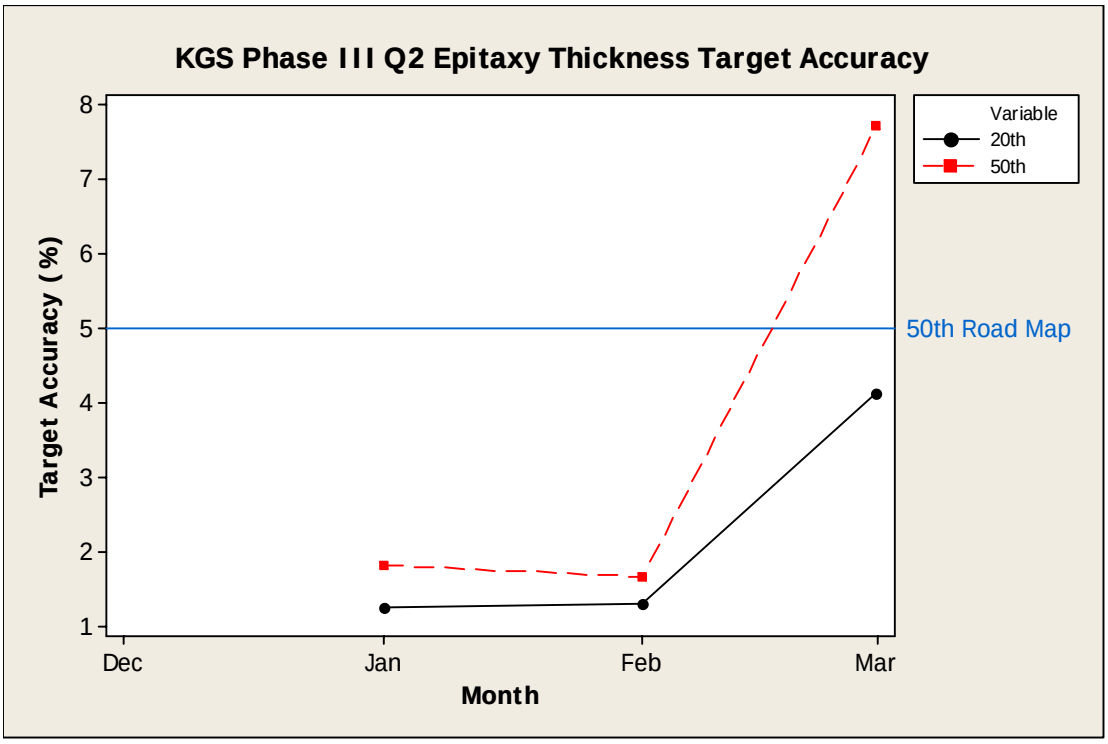

KGS Phase III Q2 Epitaxy Doping Target Accuracy
Target Accuracy (%)
20
15
10
5
0
Dec
Jan
Feb
Mar
Month
Variable
20th
50th
50th Goal
20th Goal
50th Road Map
20th Road Map


KGS Phase III Q2 Epitaxy Doping Variation within Wafer
Epitaxy Doping Variation (Max-Min/Min, %)
50
40
30
20
10
Dec
Jan
Feb
Mar
Month
Variable
20th
50th
50th Goal
50th Road Map
20th Goal
20th Road Map


KGS Phase III Q2 Equivalent Epitaxy Defect Density 4H N+ 76mm
Equivalent Epitaxy Defect Density (cm-2)
7
6
5
4
3
2
1
0
Dec
Jan
Feb
Mar
Month
Variable
20th
50th
50th Goal
20th Goal
50th Road Map
20th Road Map

New Metrics and Goals from Roadmap Discussion:





Project Milestones
Task 1: SiC Wafers Products

Highlights:

- Two wafer shipments have been completed to Rutgers, Microsemi and GeneSiC. The second set of wafers delivered to Rutgers and Microsemi were processed with DCCSS new epi process resulting in improved doping uniformity and lower defects.
- 4H SiC n+ wafers from the new SSM2 process are now available and will be used for the third lot of epiwafer deliverables.
- Expansion progress using the SSM2 process has now reached greater than 95mm. The first 100mm wafers are expected in July.

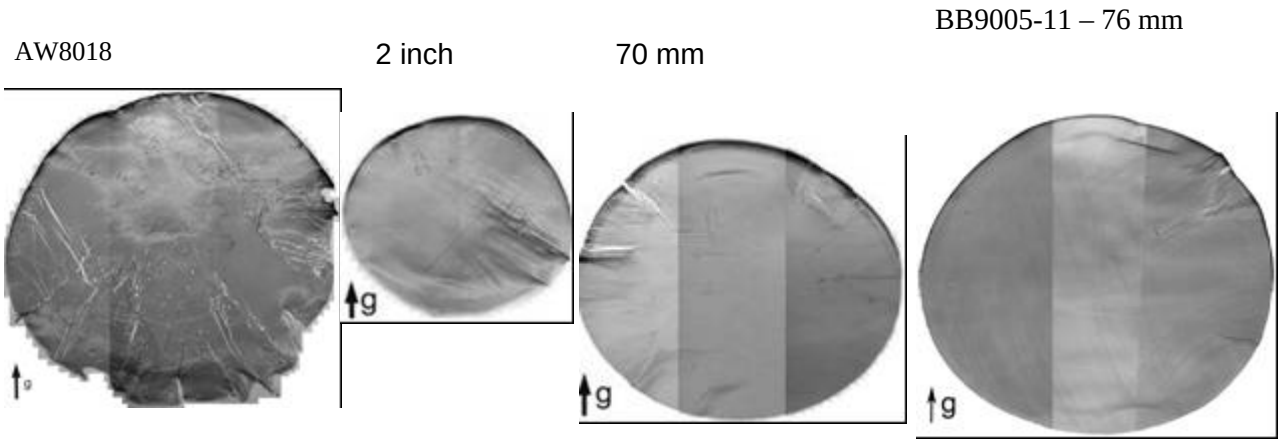
Roadblocks:

- Practice on volume processing of polishing for 100mm wafers is not yet possible. Any problems will not become visible until wafering can receive 100mm material.

Project Milestones
Task 2: Continuous Improvements in SiC Substrates

Highlights

- Diameter expansion with SSM2 method has passed 95mm. Performance is consistent with the prior diameter material.
- Optimization of resistivity in n+ 4H-SiC has delivered first SSM2 material with resistivity in the range of 0.018-0.020 ohm cm.
- X-ray topographs were carried out at SUNY on recent SSM2 growths. The resulting topographs on five different SSM2 growths have shown a step change improvement of the crystal quality. The new SSM2 process has removed the majority of the grain boundaries. The micropipe densities assessed from XRT images for all five boules have been shown to be < 0.2 cm^{-2}. Threading screw dislocations are < 1000 cm^{-2} and the overall strain is greatly reduce as shown by the shape of the reflection XRT images.



Grazing incident X-ray topographs of a typical SSM1 wafer, a 2-inch DCCS expansion wafer, a 70 mm DCCS expansion and a 76 mm DCCS expansion wafer.

Task 3. Metrology for wafer specifications

Highlights

- LLS device prediction for high voltage breakdown yield (60% of theoretical punch-through breakdown or 600V at 5 um drift layer) has been optimized. More wafer sampling from a different device fabricator makes LLS recipe statistically reliable. Now the high voltage LLS can predict yield discrepancy within 6+/-3%.
- More SLIOS data confirms extremely low stacking fault (SF) generation in DCCSS's new material (SSM-1).

Task 4. Device Technology Maturation

Highlights:

- MOS oxide breakdown failure - MOS capacitors are fabricated with PECVD oxide and NO passivation at NRL and Auburn Univ. I-V sweep shows typical Fowler-Nordheim charge injection in devices not having pre-mature breakdown. Oxide breakdown testing left burnt spots on the metal gate and those are countable. The defect density from the burnt spot is about $3x10^3/cm^2$. Site registration with image scanning and KOH etching are performed to understand underlying material defect with burnt spots. Preliminary data suggests no correlation between burnt spots in MOS capacitors and underlying material defects. This supports previous data showing no correlation between dislocations and TDDB failure spots from GE and Auburn Univ. and DCCSS oxide leakage data showing no correlation between oxide leakage current and dislocation density. These burnt spots are more likely related with particulate defects from PECVD and annealing furnace systems.

Progress toward Milestones for End of Program

Thrust	End of Quarter:	Milestone	Progress in Quarter
Task 1: SiC Wafer Products	1	Deliver 76mm diode epitaxial wafers for device fabrication	Wafers delivered.
	2	Deliver 76mm transistor epitaxial wafers for device fabrication	Wafers delivered.
	3	Deliver 100 mm diode epitaxial wafers for device fabrication	
Task 2: Continuous Improvements in SiC Substrates	3	Complete third generation development of advanced PVT/CVT methods to reduce stresses and micropipes in 4H SiC Wafers	SSM-2 wafers now put into production. 100 mm expansion work now at >95mm.
Task 3: Metrology for Wafer Specifications	1	Deliver LLS/lifetime maps for diode epitaxial wafers	Data generated
	2	Deliver LLS/lifetime maps for transistor epitaxial wafers	Data generated
	3	Deliver LLS/lifetime maps for 100mm diode epitaxial wafers for device fabrication	
Task 4: Device Technology Maturation	4	Delivery of final report on diode performance and linkage to defects, epitaxial layer metrics	
	4	Delivery of final report on transistor performance and linkage to defects, epitaxial layer metrics	
	4	Publish revised roadmap to reflect device progress	

Appendix 1: KGS Subcontractors and Quarterly Progress Points

Subcontractor	Area of Focus	Progress This Quarter
Northrup Grumman Electronics Systems	SiC-SIT full device testing	NGES reviewing recent wafer samples made with process delivering better doping uniformity.
Microsemi	High Power SiC SIT fabrication and testing	Two lots of SITs now in device fab.

GeneSiC Semiconductors	JBS Diode and normally off JFET fabrication and testing	Currently tuning Schottky metal process and implant layout.
Rutgers	Normally off VJFET fabrication and testing	First lot is now in planarization and passivation.
SUNY – Stoney Brook	Crystal Structure of SiC	Analysis of SSM2 material by XRT. Defect counts are as low as the best SiC measured.
Arizona State University	SiC Oxides, carrier lifetime and device failure analysis	
Auburn University	Growth and characterization of oxides on SiC	First group of MOSCAP samples completed Fab and will be tested at Auburn and ASU
Purdue University	High current testing and modeling of SiC diodes	Testing of PiN diodes from KGS II has started.
Carnegie Mellon University	Crystal growth parameters which impact mobility and ohmic contact formation	
Fluxtrol	Modeling and design of high uniformity induction heating systems	
NRL	Stress and reliability testing	Completed 100 hrs of 200C testing on Microsemi JBS diodes; diodes are stable.

Milestones at End of Program (no progress to report for Q2)

- Generational improvement of 4H SiC wafer crystal quality summarized by XRT and MPD analysis
- General impact of crystal mosaicity and diode performance
- Assessment of oxide quality for 76mm/100mm 4H epiwafers at different substrate orientations
- Pareto of materials defect impact by unit process in JFET fabrication
- SiC materials parameter assessed as most important for JFET performance improvements based on wafer probe data (Roadmap input – Microsemi, NGES, Rutgers, GeneSiC)
- Product device level qualification testing performance of 4H SiC in SIT process (NGES)
- SiC materials parameter assessed as most important for performance improvements in devices with p- epilayers based on wafer probe data (Roadmap input – GeneSiC, others)
- SiC materials parameter assessed as most important for JBS diode performance improvements based on wafer probe data (Roadmap input - GeneSiC)